ABSTRACT OF THE DISCLOSURE

In performing a read operation or a write operation in a memory cell, a row control circuit is first operated to activate a word line. Subsequently, a command control circuit receives a column operation command in synchronization with a clock signal so as to operate a column control circuit. Here, under the control of a timing adjusting circuit, the column control circuit starts operating a predetermined delay time after the reception of the column operation command. By delaying the operation of the column control circuit, the read operation or the write operation in the memory cell can be performed at the optimum timing corresponding to the operating timing of an internal circuit independent of the cycle of the clock signal. As a result, the number of times in receiving commands per unit time can be increased to enhance the bus occupation rate of data. Since the column control circuit is operated at the optimum timing corresponding to the operating timing of the internal circuit, a read cycle time and a write cycle time can be shortened.